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PATENT APPLICATION

NITROUS OXIDE ANNEAL OF TEOS/OZONE CVD FOR IMPROVED GAPFILL

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CROSS-REFERENCES TO RELATED APPLICATIONS

- 5 **[0001]** This application is a continuation-in-part of and claims the benefit of co-pending, commonly assigned U.S. Patent Application No. 10/247,672, entitled, "METHOD USING TEOS RAMP-UP DURING TEOS/OZONE CVD FOR IMPROVED GAP FILL," filed on September 19, 2002, by Nitin K. Ingle, *et al.*, the entire disclosure of which is herein incorporated by reference for all purposes.

10 **BACKGROUND OF THE INVENTION**

- [0002]** The fabrication sequence of integrated circuits often includes several patterning processes. The patterning processes may define a layer of conductors, such as a patterned metal or polysilicon layer, or may define isolation structures, such as trenches. In many cases the trenches are filled with an insulating, or dielectric, material. This insulating material can
15 serve several functions. For example, in some applications the material serves to both electrically isolate one region of the IC from another, and electrically passivate the surface of the trench. The material also typically provides a base for the next layer of the semiconductor to be built upon.

- [0003]** After patterning a substrate, the patterned material is not flat. The topology of the
20 pattern can interfere with or degrade subsequent wafer processing. It is often desirable to create a flat surface over the patterned material. Several methods have been developed to create such a flat, or "planarized", surface. Examples include depositing a conformal layer of material of sufficient thickness and polishing the wafer to obtain a flat surface, depositing a conformal layer of material of sufficient thickness and etching the layer back to form a
25 planarized surface, and forming a layer of relatively low-melting point material, such as doped silicon oxide, and then heating the wafer sufficiently to cause the doped silicon oxide to melt and flow as a liquid, resulting in a flat surface upon cooling. Each process has attributes that make that process desirable for a specific application.

[0004] As semiconductor design has advanced, the feature size of the semiconductor devices has dramatically decreased. Many circuits now have features, such as traces or trenches, less than a micron across. While the reduction in feature size has allowed higher device density, more chips per wafer, more complex circuits, lower operating power consumption and lower cost among other benefits, the smaller geometries have also given rise to new problems, or have resurrected problems that were once solved for larger geometries.

[0005] An example of the type of manufacturing challenge presented by sub-micron devices is the ability to completely fill a narrow trench in a void-free manner. To fill a trench with silicon oxide, a layer of silicon oxide is first deposited on the patterned substrate. The silicon oxide layer typically covers the field, as well as walls and bottom of the trench. If the trench is wide and shallow, it is relatively easy to completely fill the trench. As the trench gets narrower and the aspect ratio (the ratio of the trench height to the trench width) increases, it becomes more likely that the opening of the trench will "pinch off".

[0006] Pinching off a trench may trap a void within the trench. Under certain conditions, the void will be filled during a reflow process, for example where the deposited silicon oxide is doped and experiences viscous flow at elevated temperatures. However, as the trench becomes narrower, it becomes more likely that the void will not be filled during the reflow process. Moreover, several types of applications call for the deposition of undoped silicon oxide (sometimes referred to as undoped silicate glass, "USG"), which is difficult to reflow even at elevated temperature. Voids resulting from pinching-off are undesirable as they can reduce the yield of good chips per wafer and the reliability of the devices.

[0007] One possible solution to this problem is a two-step process wherein a first deposition step is performed under process conditions with a low (silicon-containing gas):(oxidizing gas) ratio and low deposition rate for achieving the desired gap-fill. After this first step is performed, the flow of silicon-containing process gas to the chamber is interrupted, and then a second distinct deposition step is performed under different conditions with a high (silicon-containing gas):(oxidizing gas) ratio and a high deposition rate for bulk fill. However, such a two-step process may exhibit reduced throughput due to the extended time required in the first step, and also the time consumed in halting the process gas flow and changing the apparatus configuration between the first and second steps.

[0008] Therefore, it is desirable to be able to fill narrow gaps with dielectric material in a void-free manner. It is also desirable that the process used to deposit the dielectric material be efficient, reliable, and result in high yield of devices.

BRIEF SUMMARY OF THE INVENTION

5 [0009] Embodiments of the invention thus provide a method of filling a gap defined by adjacent raised features on a substrate. The method includes providing a flow of a silicon-containing processing gas to a chamber housing the substrate and providing a flow of an oxidizing gas to the chamber. The method also includes depositing a first portion of a film as a substantially conformal layer in the gap by causing a reaction between the silicon-
10 containing processing gas and the oxidizing gas. Depositing the conformal layer includes varying over time a ratio of the (silicon-containing processing gas):(oxidizing gas) and regulating the chamber to a pressure in a range from about 200 torr to about 760 torr throughout deposition of the conformal layer. The method also includes depositing a second portion of the film as a bulk layer. Depositing a second portion of the film includes
15 maintaining the ratio of the (silicon-containing processing gas):(oxidizing gas) substantially constant throughout deposition of the bulk layer and regulating the chamber to a pressure in a range from about 200 torr to about 760 torr throughout deposition of the bulk layer. The method also includes exposing the substrate to nitrous oxide at a temperature less than about 900°C to anneal the deposited film. In some embodiments, exposing the substrate to nitrous
20 oxide at a temperature less than about 900°C to anneal the deposited film includes exposing the substrate to nitrous oxide at a temperature less than about 750°C to anneal the deposited film.

[0010] In other embodiments a method of forming a silicon oxide layer on a substrate. The method includes providing a flow of a silicon-containing processing gas to a chamber
25 housing the substrate and providing a flow of an oxidizing processing gas to the chamber. The method also includes causing a reaction between the silicon-containing processing gas and the oxidizing processing gas to form a silicon oxide layer. The method further includes heating the substrate in the presence of nitrous oxide. In some aspects, providing a flow of a silicon-containing processing gas comprises providing a flow of tetraethylorthosilicate
30 (TEOS). In some aspects providing a flow of an oxidizing processing gas comprises providing a flow of ozone. Causing a reaction between the silicon-containing processing gas and the oxidizing processing gas may include regulating the pressure of the chamber to sub-atmospheric levels. The sub-atmospheric levels may include pressures in a range from about

200 torr to less than about 760 torr. Causing a reaction between the silicon-containing processing gas and the oxidizing processing gas may include regulating the temperature of the chamber to a range from about 400° C to about 570° C. In some aspects heating the substrate in the presence of nitrous oxide may include heating the substrate to a temperature
5 in a range from about 750° C to about 1000° C in a furnace. This also may include introducing steam into the furnace. Heating the substrate in the presence of nitrous oxide also may include heating the substrate to a temperature greater than or equal to 1000° C in a rapid thermal process for a duration greater than or equal to 1 minute.

[0011] In other embodiments, a method of forming a silicon oxide layer on a substrate
10 includes providing a flow of a silicon-containing processing gas to a chamber housing the substrate and providing a flow of ozone to the chamber. The method also includes causing a reaction between the silicon-containing processing gas and the ozone to form a silicon oxide layer. The method also includes heating the substrate in the presence of nitrous oxide in a furnace to a temperature in the range from about 750° C to about 1000° C. The method may
15 include introducing steam into the furnace. The silicon-containing processing gas may include tetraethylorthosilicate (TEOS).

[0012] In still other embodiments a method of forming a silicon oxide layer on a substrate, includes providing a flow of tetraethylorthosilicate (TEOS) processing gas to a chamber housing the substrate, providing a flow of ozone to the chamber, and regulating the pressure
20 of the chamber to a pressure in a range from about 200 torr to less than about 760 torr. The method further includes causing a reaction between the TEOS and the ozone to form a silicon oxide layer. The method also includes heating the substrate in the presence of nitrous oxide. In some aspects heating the substrate in the presence of nitrous oxide includes heating the substrate in the presence of nitrous oxide in a furnace to a temperature in the range from
25 about 750° C to about 1000° C. In other aspects heating the substrate in the presence of nitrous oxide includes heating the substrate to a temperature greater than or equal to 1000° C in a rapid thermal process for a duration greater than or equal to 1 minute.

[0013] In yet other embodiments a method of forming a silicon oxide layer on a substrate includes providing a flow of tetraethylorthosilicate (TEOS) processing gas to a chamber
30 housing the substrate, providing a flow of ozone to the chamber, regulating the pressure of the chamber to a pressure in the range from about 200 torr to less than about 760 torr, and causing a reaction between the TEOS and the ozone to form a silicon oxide layer. The

method also includes heating the substrate in the presence of nitrous oxide in a furnace to a temperature in the range from about 750° C to about 1000° C.

BRIEF DESCRIPTION OF THE DRAWINGS

- 5 [0014] A further understanding of the nature and advantages of the present invention may be realized by reference to the remaining portions of the specification and the drawings wherein like reference numerals are used throughout the several drawings to refer to similar components.
- [0015] Fig. 1 shows a simplified cross-sectional view of a trench filled with oxide utilizing
10 conventional deposition techniques.
- [0016] Fig. 2A shows a simplified cross-sectional view of a second trench filled with oxide utilizing conventional deposition techniques.
- [0017] Fig. 2B shows a simplified cross-sectional view of the conventional oxide-filled trench of Fig. 2A after a chemical mechanical polishing.
- 15 [0018] Fig. 3 shows a simplified cross-sectional view of an oxide-filled trench in accordance with an embodiment of the present invention.
- [0019] Fig. 4 illustrates a method according to an embodiment of the invention.
- [0020] Fig. 5A is a simplified representation of a CVD apparatus according to embodiments of the present invention.
- 20 [0021] Fig. 5B is a simplified representation of the user interface for a CVD system in relation to a deposition chamber in a multi-chamber system.
- [0022] Fig. 5C is a simplified diagram of a gas panel and supply lines in relation to a deposition chamber.
- [0023] Fig. 6 is a simplified cross section of a portion of an integrated circuit according to
25 embodiments of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0024] Embodiments of the present invention provide methods, apparatuses, and devices related to chemical vapor deposition of silicon oxide. In one embodiment, a process is used to efficiently form a silicon oxide layer with good gap-filling properties. During a deposition

phase of the process, silicon-containing gas and oxidizing processing gas are flowed, resulting in the formation of silicon oxide exhibiting a highly conformal character. During an annealing phase utilizing Nitrous Oxide (N_2O), potential weak seams or voids created during the deposition process are strengthened. Aspects of the present invention are best understood with reference to the limitations of conventional processes.

I. Introduction

[0025] Fig. 1 shows a simplified cross-sectional view of an example of trench 100 filled with silicon oxide 102 deposited utilizing a conventional process. Fig. 1 shows that the increased rate of deposition of oxide material on the raised edges of the trench 100 has resulted in pinching-off of the trench and created unwanted void or pinhole defect 104 within the feature. Void 104 can adversely affect the operation of a semiconductor device that is relying upon the consistent dielectric strength of the oxide-filled trench.

[0026] Fig. 1 also shows formation of bulk oxide layer 106 over oxide-filled trench 100. Bulk layer 106 provides additional dielectric material to serve as the starting point for continued processing, for example subsequent chemical-mechanical polishing. Although bulk layer 106 overlies the oxide-filled trench and is substantially planar, subsequent processing may expose the void 104.

[0027] Fig. 2A shows a simplified cross-sectional view of another example of a trench 200 filled with silicon oxide deposited utilizing a conventional process. Fig. 2A shows that while pinch-off and void formation has not occurred, weak seam 202 is formed where silicon oxide material 204, grown outward from opposed sidewalls 200a of trench 200, meets.

[0028] The relatively poor quality of seam 202 results in oxide along this seam being removed at faster rates relative to the surrounding oxide material when the oxide layer is exposed to an etchant such as hydrofluoric acid (HF). Fig. 2B shows a simplified cross-sectional view of the oxide-filled trench 200 of Fig. 2A after exposure to chemical mechanical polishing (CMP) and post-CMP cleaning utilizing HF etchant. Fig. 2B illustrates that the enhanced rate of etching along seam 202 has resulted in unwanted dishing 208 in the surface of the oxide-filled trench 200. Such dishing 208 can adversely affect operation of a semiconductor device relying upon the consistent dielectric strength of the oxide-filled trench feature.

[0029] Figs. 1 and 2A-B are to be contrasted with Fig. 3, which shows a simplified cross-sectional view of an oxide-filled trench structure formed utilizing an embodiment of a process in accordance with the present invention. Specifically, a silicon-containing gas such as TEOS and an oxidizing processing gas such as ozone are flowed during a deposition process, followed by thermal annealing using N_2O . This process results in formation of an oxide film 300 that includes a highly conformal initial layer 300b proximate to the surrounding silicon sidewalls, and a less-conformal bulk layer 300a which fills the remaining volume of the trench 302. More importantly, however, the oxide-filled trench 302 of Fig. 3 does not include the voids or weak seams associated with similar features formed utilizing the conventional oxide CVD processes previously described.

II. An Exemplary Oxide Deposition Process

[0030] Fig. 4 illustrates an exemplary method 400 according to embodiments of the invention. At block 402, an oxide layer is deposited on a substrate in a CVD process, and at block 404 the oxide layer is annealed. The deposition may take place in a CVD chamber, which is described in detail hereinafter. The deposition includes flowing a silicon-containing process gas into a chamber that houses the substrate at block 406 and flowing an oxidizing processing gas into the chamber at block 408. In a specific embodiment, the silicon-containing gas comprises tetraethylorthosilicate (TEOS); however, other silicon-containing processing gases such as SiH_4 , S_2H_6 , S_3H_8 , etc., may be used. Also in a specific embodiment, the oxidizing processing gas comprises ozone (O_3), although oxidizing gases such as O_2 , H_2O , H_2O_2 may alternatively be used. Furthermore, this embodiment of the invention is described for gapfill with an USG, but it will be appreciated that the film may be doped in alternative embodiments. For example, dopants may be added to the film by including a precursor gas with the desired dopant, such as by including a flow of SiF_4 to fluorinate the film, including a flow of PH_3 to phosphorate the film, including a flow of B_2H_6 to boronate the film, including a flow of N_2 to nitrogenate the film, and the like.

[0031] The chamber pressure during the deposition process of block 402 may be regulated as indicated by block 410. In some embodiments, the pressure is maintained at sub-atmospheric pressures. In a specific embodiment, the pressure during the deposition process may range from about 200 torr to less than about 760 torr, although the pressure profile may remain within a much narrower range. Also during the deposition process, the temperature may be regulated as indicated by block 412. In some embodiments the temperature is varied

from about 400° C to about 570° C, although the temperature may be maintained within a much narrower range. Regulating the temperature and pressure of the chamber regulates a reaction between the silicon-containing process gas and the oxidizer-containing process gas.

[0032] Oxide layer deposition 402 may be performed according to the process described in more detail in previously-incorporated U.S. Patent Application No. 10/247,672. The process includes varying the ratio (silicon-containing gas):(oxidizer-containing gas) 414, thereby varying the rate at which the oxide layer is deposited and possibly the composition of the conformal layer. For example, at the start of the process the concentration of the silicon-containing gas in the mixture may be small, then may be increased as the film thickness increases. In such examples, oxide layer deposition 402 may comprise depositing a conformal initial layer 300b during a phase in which the silicon-containing gas concentration in the mixture is small, then depositing a bulk layer 300a during a phase in which the silicon-containing gas concentration in the mixture is higher.

[0033] Oxide layer deposition 402 may comprise an SACVD process. With high aspect ratio narrow gaps, greater success is achieved by varying the ratio (silicon-containing process gas):(oxidizing gas), beginning with a lower concentration of silicon-containing process gas, as described above, for gapfill. The process may be further aided by disbursing the gas uniformly across the substrate. As the concentration of silicon-containing process gas in the mixture increases, the gas may be disbursed closer to the surface of the substrate. This technique and an apparatus for practicing it are more fully described in co-pending, commonly assigned U.S. Patent Application No. 10/057,280, filed on January 25, 2002, entitled "GAS DISTRIBUTION SHOWERHEAD," and/or co-pending, commonly assigned U.S. Patent Application No. 10/674,569, filed on September 29, 2003, entitled "GAS DISTRIBUTION SHOWERHEAD," the entire disclosure of each of which are herein incorporated by reference.

[0034] Following the deposition process, the oxide layer is annealed at block 404. The annealing process includes heating the substrate and flowing N₂O into the chamber or furnace. This is shown as block 416. The N₂O interacts with the SiO₂ network at high temperatures and strengthens any weak seams formed during the deposition process. The resulting SiO₂ layer is seam-free and suited for CMP.

[0035] Annealing may take place *in situ* or *ex situ*. For example, if oxide layer deposition 402 takes place in a CVD chamber, annealing 404 may take place in the same

chamber immediately thereafter. Annealing 404 alternatively may take place in another chamber of a multi-chamber system or in a different chamber system (e.g., a furnace). In some embodiments, annealing comprises a Rapid Thermal Process (RTP) as more fully described in U.S. Patent No. 5,660,472, the entire disclosure of which is herein incorporated
5 by reference for all purposes. The annealing process may be wet (e.g., using steam), as indicated by block 418, or dry.

[0036] The annealing temperature may range from about 750° C to about 1000° C for furnace anneal and up to about 1200° C for RTP anneal. The annealing duration is temperature dependent and may range from about 10 minutes to around 2 hours for furnace
10 anneal and as few as 5 seconds up to around 3 minutes for RTP. As a result, in most cases, the layer is annealed by restructuring the SiO₂ network without exceeding the USG reflow temperature.

[0037] During the N₂O anneal process, a thin layer of silicon nitride and/or silicon oxynitride may be formed in the SiO₂/Si interface. This layer may prevent further oxidation
15 into the Si in which the trench is formed. This is particularly useful for wet anneal processes since the water vapor may otherwise penetrate into the Si layer, leading to excessive oxidation. Another advantage to the N₂O anneal process is that it provides integrity of the top corners of STI trenches.

[0038] Alternative embodiments of the previously-described processes may include more
20 or fewer operations. Further, the operations in alternative embodiments are not necessarily performed in the order depicted, as is apparent to those skilled in the art in light of the disclosure herein.

III. An Exemplary Deposition System

[0039] Having described methods according to embodiments of the present invention,
25 attention is directed to Fig. 5A, which illustrates a simplified diagram of a CVD system 510 according to an embodiment of the present invention. This system is suitable for performing thermal, SACVD processes, as well as other processes, such as reflow, drive-in, cleaning, etching, and gettering processes. Multiple-step processes can also be performed on a single substrate or wafer without removing the substrate from the chamber. The major components
30 of the system include, among others, a vacuum chamber 515 that receives process and other gases from a gas delivery system 589, a vacuum system 588, a remote microwave plasma

system 555, and a control system 553. These and other components are described below in order to understand the present invention.

[0040] The CVD apparatus 510 includes an enclosure assembly 512 housing a vacuum chamber 515 with a gas reaction area 516. A gas distribution plate 520 is provided above the gas reaction area 516 for dispersing reactive gases and other gases, such as purge gases, through perforated holes in the gas distribution plate 520 to a wafer (not shown) that rests on a vertically movable heater 525 (also referred to as a wafer support pedestal). The heater 525 can be controllably moved between a lower position, where a wafer can be loaded or unloaded, for example, and a processing position closely adjacent to the gas distribution plate 520, indicated by a dashed line 513, or to other positions for other purposes, such as for an etch or cleaning process. A center board (not shown) includes sensors for providing information on the position of the wafer.

[0041] In some embodiments, the gas distribution plate 520 may be of the variety described in either of previously-incorporated U.S. Patent Application Serial Nos. 10/057,280 or 10/674,569. These plates improve the uniformity of gas disbursement at the substrate and are particularly advantageous in deposition processes that vary gas concentration ratios. In some examples, the plates work in combination with the vertically moveable heater 525 (or moveable wafer support pedestal) such that deposition gases are released farther from the substrate when the ratio is heavily skewed in one direction (*e.g.*, when the concentration of a silicon-containing gas is small compared to the concentration of an oxidizer-containing gas) and are released closer to the substrate as the concentration changes (*e.g.*, when the concentration of silicon-containing gas in the mixture is higher). In other examples, the orifices of the gas distribution plate are designed to provide more uniform mixing of the gases.

[0042] The heater 525 includes an electrically resistive heating element (not shown) enclosed in a ceramic. The ceramic protects the heating element from potentially corrosive chamber environments and allows the heater to attain temperatures up to about 800°C. In an exemplary embodiment, all surfaces of the heater 525 exposed to the vacuum chamber 515 are made of a ceramic material, such as aluminum oxide (Al_2O_3 or alumina) or aluminum nitride.

[0043] Reactive and carrier gases are supplied through the supply line 543 into a gas mixing box (also called a gas mixing block) 527, where they are preferably mixed together

and delivered to the gas distribution plate 520. The gas mixing box 527 is preferably a dual input mixing block coupled to a process gas supply line 543 and to a cleaning/etch gas conduit 547. A valve 528 operates to admit or seal gas or plasma from the gas conduit 547 to the gas mixing block 527. The gas conduit 547 receives gases from an integral remote microwave plasma system 555, which has an inlet 557 for receiving input gases. During deposition processing, gas supplied to the plate 520 is vented toward the wafer surface (as indicated by arrows 521), where it may be uniformly distributed radially across the wafer surface, typically in a laminar flow.

[0044] Purging gas may be delivered into the vacuum chamber 515 from the plate 520 and/or an inlet port or tube (not shown) through the bottom wall of enclosure assembly 512. The purging gas flows upward from the inlet port past the heater 525 and to an annular pumping channel 540. An exhaust system then exhausts the gas (as indicated by arrows 522) into the annular pumping channel 540 and through an exhaust line 560 to a vacuum system 588, which includes a vacuum pump (not shown). Exhaust gases and entrained particles are drawn from the annular pumping channel 540 through the exhaust line 560 at a rate controlled by a throttle valve system 563.

[0045] The remote microwave plasma system 555 can produce a plasma for selected applications, such as chamber cleaning or etching native oxide or residue from a process wafer. Plasma species produced in the remote plasma system 555 from precursors supplied via the input line 557 are sent via the conduit 547 for dispersion through the plate 520 to the vacuum chamber 515. Precursor gases for a cleaning application may include fluorine, chlorine, and other reactive elements. The remote microwave plasma system 555 also may be adapted to deposit plasma-enhanced CVD films by selecting appropriate deposition precursor gases for use in the remote microwave plasma system 555.

[0046] The system controller 553 controls activities and operating parameters of the deposition system. The processor 550 executes system control software, such as a computer program stored in a memory 570 coupled to the processor 550. Preferably, the memory 570 may be a hard disk drive, but of course the memory 570 may be other kinds of memory, such as read-only memory or flash memory. In addition to a hard disk drive (e.g., memory 570), the CVD apparatus 510 in a preferred embodiment includes a floppy disk drive and a card rack (not shown).

[0047] The processor 550 operates according to system control software programmed to operate the device according to the methods disclosed herein. For example, sets of instructions may dictate the timing, mixture of gases, chamber pressure, chamber temperature, microwave power levels, susceptor position, and other parameters of a particular process. Other computer programs such as those stored on other memory including, for example, a floppy disk or another computer program product inserted in a disk drive or other appropriate drive, may also be used to operate the processor 550 to configure the CVD system 510 into various apparatus.

[0048] The processor 550 has a card rack (not shown) that contains a single-board computer, analog and digital input/output boards, interface boards and stepper motor controller boards. Various parts of the CVD system 510 conform to the Versa Modular European (VME) standard which defines board, card cage, and connector dimensions and types. The VME standard also defines the bus structure having a 16-bit data bus and 24-bit address bus.

[0049] Fig. 5B is a simplified diagram of a user interface in relation to the CVD apparatus chamber 530. The CVD apparatus 510 includes one chamber of a multichamber system. Wafers may be transferred from one chamber to another for additional processing. In some cases the wafers are transferred under vacuum or a selected gas. The interface between a user and the processor is via a CRT monitor 573a and a light pen 573b. A mainframe unit 575 provides electrical, plumbing, and other support functions for the CVD apparatus 510. Exemplary mainframe units compatible with the illustrative embodiment of the CVD apparatus are currently commercially available as the PRECISION 5000™, the CENTURA 5200™, and the PRODUCER SE™ systems from APPLIED MATERIALS, INC. of Santa Clara, California.

[0050] In some embodiments two monitors 573a are used, one mounted in the clean room wall 571 for the operators, and the other behind the wall 572 for the service technicians. Both monitors 573a simultaneously display the same information, but only one light pen 573b is enabled. The light pen 573b detects light emitted by the CRT display with a light sensor in the tip of the pen. To select a particular screen or function, the operator touches a designated area of the display screen and pushes the button on the pen 573b. The touched area changes its highlighted color, or a new menu or screen is displayed, confirming communication between the light pen and the display screen. Of course, other devices, such

as a keyboard, mouse, or other pointing or communication device, may be used instead of or in addition to the light pen 573b to allow the user to communicate with the processor.

[0051] Fig. 5C illustrates a general overview of an embodiment of the CVD apparatus 510 in relation to a gas supply panel 580 located in a clean room. As discussed above, the CVD system 510 includes a chamber 515 with a heater 525, a gas mixing box 527 with inputs from an inlet tube 543 and a conduit 547, and remote microwave plasma system 555 with input line 557. As mentioned above, the gas mixing box 527 is for mixing and injecting deposition gas(es) and clean gas(es) or other gas(es) through the inlet tube 543 to the processing chamber 515.

[0052] The remote microwave plasma system 555 is integrally located and mounted below the chamber 515 with the conduit 547 coming up alongside the chamber 515 to the gate valve 528 and the gas mixing box 527, located above the chamber 515. Microwave generator 511 and ozonator 551 are located remote from the clean room. Supply lines 583 and 585 from the gas supply panel 580 provide reactive gases to the gas supply line 543. The gas supply panel 580 includes lines from gas or liquid sources 590 that provide the process gases for the selected application. The gas supply panel 580 has a mixing system 593 that mixes selected gases before flow to the gas mixing box 527. In some embodiments, gas mixing system 593 includes a liquid injection system for vaporizing reactant liquids such as tetraethylorthosilicate ("TEOS"), triethylborate ("TEB"), and triethylphosphate ("TEPO").

Vapor from the liquids is usually combined with a carrier gas, such as helium. Supply lines for the process gases may include (i) shut-off valves 595 that can be used to automatically or manually shut off the flow of process gas into line 585 or line 557, and (ii) liquid flow meters (LFM) 501 or other types of controllers that measure the flow of gas or liquid through the supply lines.

[0053] As an example, a mixture including TEOS as a silicon source may be used with gas mixing system 593 in a deposition process for forming a silicon oxide film. The TEPO is a liquid source that may be vaporized by conventional boiler-type or bubbler-type hot boxes. However, a liquid injection system is preferred as it provides greater control of the volume of reactant liquid introduced into the gas mixing system. The liquid is typically injected as a fine spray or mist into the carrier gas flow before being delivered to a heated gas delivery line 585 to the gas mixing block and chamber. One or more sources, such as oxygen (O₂) or ozone (O₃) flow to the chamber through another gas delivery line 583, to be combined with

the reactant gases from heated gas delivery line 585 near or in the chamber. Of course, it is recognized that other sources of dopants, silicon, and oxygen also may be used.

IV. Exemplary Semiconductor Structure

[0054] Fig. 6 illustrates a simplified cross-sectional view of an integrated circuit 700 according to an embodiment of the present invention. As shown in Fig. 7, the integrated circuit 700 includes NMOS and PMOS transistors 703 and 706, which are separated and electrically isolated from each other by oxide-filled trench isolation structure 720.

Alternatively, field oxide isolation can be used to isolate devices, or a combination of isolation techniques may be used. Each of the transistors 703 and 706 comprises a source region 712, a gate region 715, and a drain region 718.

[0055] A premetal dielectric (PMD) layer 721 separates the transistors 703 and 706 from the metal layer 740, with connections between metal layer 740 and the transistors made by contacts 724. The premetal dielectric layer 721 may comprise a single layer or multiple layers. The metal layer 740 is one of four metal layers, 740, 742, 744, and 746, included in the integrated circuit 700. Each metal layer is separated from adjacent metal layers by intermetal dielectric layers 727, 728, and 729. Adjacent metal layers are connected at selected openings by vias 726. Planarized passivation layers 730 are deposited over the metal layer 746.

[0056] A silicon oxide layer deposited according to an embodiment of the present invention may be used to form one or more of the dielectric layers shown in integrated circuit 700. For example, a silicon oxide layer may be used to create trench isolation structure 720. A silicon oxide layer deposited according to the present invention may also be used to create PMD layer 721, or the higher layer intermetal dielectric layers 727-729 of the overlying interconnect structure.

[0057] A silicon oxide layer deposited according to an embodiment of the present invention may also be used in damascene layers, which are included in some integrated circuits. In damascene layers, a blanket layer is deposited over a substrate, selectively etched through to the substrate, and then filled with metal and etched back or polished to form metal contacts 724. After the metal layer is deposited, a second blanket deposition is performed and selectively etched. The etched areas are then filled with metal and etched back or polished to form vias 726.

[0058] It should be understood that the simplified integrated circuit 700 is for illustrative purposes only. One of ordinary skill in the art could implement the present method for fabrication of other integrated circuits, such as microprocessors, application-specific integrated circuits (ASICs), memory devices, and the like.

5 **[0059]** Having described several embodiments, it will be recognized by those of skill in the art that various modifications, alternative constructions, and equivalents may be used without departing from the spirit of the invention. Additionally, a number of well known processes and elements have not been described in order to avoid unnecessarily obscuring the present invention. Accordingly, the above description should not be taken as limiting the scope of
10 the invention, which is defined in the following claims.